M.TECH IN ECE-(VLSI DESIGN)
(REGULAR)

SEMESTER I

Subject Code	Name of Subject	Teaching Period			Credit Points
		L	T	P	
01MVL-101	VLSI Technology	4	1	0	5
01MVL-102	MOS Circuit Design	4	1	0	5
01MVL-103	Digital signal processing	4	1	0	5
01MVL-104	Digital System Design	4	1	0	5
Practical/Viva-voice					
01MVL-201	VHDL circuit design lab	0	0	3	2
01MVL-301	Discipline & Co-Curricular activities	0	0	4	1
GRAND TOTAL		16	4	7	23

SEMESTER II

Subject Code	Name of Subject	Teaching Period			Credit Points
		L	T	P	
02MVL-101	Analog VLSI Design	4	1	0	5
02MVL-102	Embedded System Design	4	1	0	5
02MVL-103	CMOS RF Circuit Design	4	1	0	5
02MVL-104	VLSI Test & Testability	4	1	0	5
Practical/Viva-voice					
02MVL-201	Wireless communication lab	0	0	3	2
02MVL-301	Discipline & Co-Curricular activities	0	0	4	1
GRAND TOTAL		16	4	7	23

SEMESTER III

Subject Code	Name of Subject	Teaching Period			
		L	T	P	Credit
03MVL-101	Algorithms for VLSI Design Automation	4	1	0	5
03MVL-102	Process, Devices & Circuit Simulation	4	1	0	5
03MVL-201	Project work	5	0	0	5
03MVL-203	Seminar	3	0	0	3
03MVL-301	Discipline & Co-Curricular activities	0	0	4	1
GRAND TOTAL		16	2	4	19

SEMESTER IV

Subject code	Name of Subject	TEACHING PERIODS			Credit Points
		L	T	P	
04MVL 201	DISSERTATION: CONTINOUS EVALUATION	5	0	0	5
	PROJECT REPORT	6	0	0	6
	VIVA VOICE	6	0	0	6
06MVL 301PT	DISCIPLINE & EXTRA CURRICULAR ACTIVITIES	0	0	4	1
	Total	17	0	4	18

VLSI TECHNOLOGY

Course/Paper: 01MVL-101
MVL Semester-I

Crystal growth & wafer preparation. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc. **Epitaxy**
Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

Oxidation
Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides. Oxides. Oxidation technique & systems dry & wet oxidation. Masking properties of SiO2

Diffusion
Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer. **Lithography**
Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X ray sources & masks. Ion lithography.

Etching
Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching,

References:

1. Sze," Modern Semiconductor Device Physics", John Wiley & Sons, 2000. B.G. Streetman,
2. "Solid State Electronics Devices", Prentice Hall, 2002Chen, "VLSI Technology" Wiley, March2003.

MOS CIRCUIT DESIGN

Course/Paper: 01MVL-102
MVL Semester-I

Introduction:
Basic principle of MOS transistor, Introduction to large signal MOS models (longchannel) for digital design.

The MOS Inverter:
Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption.

MOS Circuit Layout & Simulation:
MOS SPICE model, device characterization, Circuit characterization, interconnects simulation. MOS device layout: Transistor layout, Inverter layout, CMOS digital circuits layout & simulation

Combinational MOS Logic Design
Static MOS design: Complementary MOS, Ratio edlogic, Pass Transistor logic, complex logic circuits. **Dynamic MOS design:** Dynamic logic families and performances. **Sequential MOS Logic Design**
Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells design.

Interconnect & Clock Distribution

Interconnect delays, Cross Talks, Clock Distribution. Introduction to low power design, Input and Output Interface circuits. **BiCMOS Logic Circuits**
Introduction, BJT Structure & operation, Basic BiCMOS Circuit behavior, Switching Delay in BiCMOS Logic circuits, BiCMOS Applications.

References:

1. Kang & Leblebigi "CMOS Digital IC CircuitAnalysis & Design"- McGraw Hill, 2003
2. Rabey, "Digital Integrated Circuits Design", Pearson Education, Second Edition, 2003
3. Weste and Eshraghian, "Principles of CMOS VLSI design" Addison-Wesley, 2002

01MVL-103

DIGITAL SIGNAL PROCESSING

Course/Paper: 01MVL-103
MVL Semester-I

Discrete time signals and systems, Z-transforms, structures for digital filters, design procedures for FIR and IIR filters. Frequency transformations: linear phase design; DFT. Methods for computing FFT. Noise analysis of digital filters, power spectrum estimation.

Signals and signal Processing: characterization & classification of signals, typical Signal Processing operations, example of typical Signals, typical Signals Processing applications.

Time Domain Representation of Signals & Systems: Discrete Time Signals, Operations on Sequences, the sampling process, Discrete-Time systems, Time-Domain characterization of LTI Discrete-Time systems, state-space representation of LTI Discrete-Time systems, random signals.

Transform-Domain Representation of Signals: the Discrete-Time Fourier Transform, Discrete Fourier Transform, DFT properties, computation of the DFT of real sequences, Linear Convolution using the DFT. Z-transforms, Inverse z-transform, properties of z-transform, transform domain representations of random signals.

Transform-Domain Representation of LTI Systems: the frequency response, the transfer function, types of transfer function, minimum-phase and maximum-Phase transfer functions, complementary transfer functions, Discrete-Time processing of random signals.

Digital Processing of Continuous-Time Signals: sampling of Continuous Signals, Analog Filter Design, Anti-aliasing Filter Design, Sample-and-hold circuits, A/D & D/A converter, Reconstruction Filter Design.

Digital Filter Structure: Block Diagram representation, Signal Flow Graph Representation, Equivalent Structures, bone FIR Digital Filter Structures, IIR Filter Structures, State-space structure, all pass filters, tunable IIR Digital filters. cascaded Lattice realization of IIR and FIR filters, Parallel all pass realization of IIR transfer function, Digital Sine-Cosine generator.

Digital Filter Design: Impulse invariance method of IIR filter design, Bilinear Transform method of IIR Filter Design, Design of Digital IIR notch filters, FIR filter Design based on truncated former sens, FIR filter design based on Frequency Sampling approach. Applications of DSP.

References:

1. Sanjit K. Mitra, "Applications DSPa Computer based approach", TMH.
2. Allan Y. Oppenhein& Ronald W. Schater, "Digital Signal Processing", PHI.

01MVL-104

DIGITAL SYSTEM DESIGN

Course/Paper: 01MVL-104
MVLSemester-I

Specification of combinational systems using VHDL, Introduction to VHDL, Basic language element of VHDL, Behavioral Modeling, Data flow modeling,Structuralmodeling,Subprogramsandoverloading,VHDLdescriptionofgates.

Description and design of sequential circuits using VHDL, Standard combinational modules, Design of a Serial Adder with Accumulator, State Graph forControlNetwork,designofaBinaryMultiplier,MultiplicationofaSignedBinaryNumber,DesignofaBinaryDivider.

Register- transfer level systems, Execution Graph, Organization of System, Implementation of RTL Systems, Analysis of RTL Systems, and Design of RTL Systems.

Data Subsystems, Storage Modules, Functional Modules, Data paths, Control Subsystems, Micro programmed Controller, Structure of a micro programmed controller, Micro instruction Format, Micro instruction sequencing, Micro instruction Timing, Basic component of a micro system, memory subsystem.

I/O sub system, Processors, Operation of the computer and cycle time. Binary Decoder, Binary Encoder, Multiplexers and Demultiplexers, Floating Point Arithmetic-Representation of Floating Point Number, Floating Point Multiplication.

References:

1. J. Bhaskar,"AVHDLPrimer",AddisonWesley,1999.
2. M. Ercegovac,T. LangandL.J. Moreno, "IntroductiontoDigitalSystems",Wiley,2000
3. C. H. Roth,"Digital System Designusing VHDL",PWSPublishing
4. J.F.Wakerly,"Digital Design-Principles and Practices",PHL
5. Douglas Perry, "VHDL", MGH
6. MichaeJohnSebastianSmith,"Application-SpecificIntegratedCircuits",Addison-Wesley.
7. Z. Navabi,"VHDL-Analysis and Modeling of Digital Systems",MGH

01MVL-201

LAB-VHDL Circuit Design Lab

Course/Paper: 01MVL-201
MVLSemester-I

Design of following ckt using appropriate software like VHDL/ FPGA.

1 3 input NAND gate.
2. Half adder.
3. D-Latch.
4. Serial in-serial out shift register.
5. half subtractor
6. multiplexer.
7. Digital clock.
8. ALU

ANALOG VLSI DESIGN

Course/Paper: 02MVL-101
MVLSemester-II

Small Signal & large signal Models of MOS& BJT transistor. Analog MOS Process
(Double Poly Process)

MOS & BJT Transistor Amplifiers:
Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers

Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Active Cascode. Differential Amplifiers: Differential pair & DC transfer characteristics.

Current Mirrors, Active Loads & References
Current Mirrors: Simple current mirror, Cascode current mirrors Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques, Frequency Response,

Operational Amplifier:

Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, Bipolar operational amplifiers. Frequency response & compensation.

Nonlinear Analog Circuits:
Analysis of four quadrant and variable Tran conductance multiplier, Voltage controlled oscillator, Comparators, Analog Buffers, Source Follower and Other Structures. Phase Locked Techniques; Phase Locked Loops (PLL), closed loop analysis of PLL. Digital-to-Analog (D/A) and Analog-to-Digital (A/D)Converters

OTA & Switched Capacitor filters
OTA Amplifiers. Switched Capacitor Circuits and Switched Capacitor Filters.

References:

1. Paul B Gray and Robert G Meyer, "Analysis and Design ofAnalog Integrated Circuits".
2. Behzad Razavi, "Principles of data conversion system design", S.Chand and company Ltd, 2000. John Wiley
3. D.A. Johns and Martin,Analog Integrated Circuit Design, John Wiley, 1997.
4. R Gregorian and GC Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.
5. RL Geiger, P E Allen and NR Strader, VLSI Design Techniques for Analog & Digital Circuits, McGraw Hill, 1990.
6. Gray and Meyer," Analysis and Design of Analog IC ", Wiley international,1996.
7. Gray, Wooley, Brodersen, "Analog MOS Integrated circuits", IEEE press, 1989.
8. Kenneth R. Laker, Willy M.C. Sensen," Design ofAnalog Integrated circuits and systems", McGraw Hill, 1994.

EMBEDDED SYSTEM DESIGN

Course/Paper: 02MVL-102
MVL Semester-II

Introduction to an embedded systems design:
Introduction to Embedded system, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES.

RTOS & its overview:
Real Time Operating System: Task and Task States, tasks and data, semaphores and shared Data Operating system Services-Message queues-Timer Function-Events-Memory Management, Interrupt Routines in an RTOS environment, basic design Using RTOS.

Microcontroller:
Role of processor selection in Embedded System (Microprocessor V/s Micro-controller), 8051 Microcontroller: Architecture, basic assembly language programming concepts, Instruction set, Addressing Modes, Logical Operation, Arithmetic Operations, Subroutine, Interrupt handling, Timing subroutines, Serial data transmission, Serial data communication

Embedded system development
Embedded system evolution trends. Round - Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms. Introduction to-assembler-compiler-cross compilers and Integrated Development Environment (IDE). Object Oriented Interfacing, Recursion, Debugging strategies, Simulators.

Networks for Embedded Systems
The I2C Bus, The CAN bus, SHARC link Ports, Ethernet, Myrinet, Internet, Introduction to Bluetooth: Specification, Core Protocol, Cable replacement protocol. IEEE 1149.1 (JTAG) Testability: Boundary Scan Architecture.

References:

1. Embedded Systems by Raj Kamal, TMH
2. The8051 Microcontroller by K.J.Ayala, Penram International
3. J B Peatman, Design with PIC Microcontrollers, Prentice Hall
4. An Embedded Software Primer by David E. Simon, Pearson Education
5. Designing Embedded Hardware by John Catsoulis, O'reilly
6. Embedded System Design by FrankVahid, Tony Givargis,", John Wiley & Sons, Inc
7. Building Embedded Linux Systems by Karim Yaghmour, O'reilly
8. Programming Embedded Systems by Michael Barr, O'reilly
9. Real-time systems & software by Alan C. Shaw, John Wiley & sons, Inc.
10. Computers as Components by Wayne Wolf, Harcourt India Pvt. Ltd.

11. Embedded System Design by Peter Marwedel, KluwerAcadeemic Pub.
12. Programming and Customizing the AVR Microcontroller by Dhananjay Gadre, MGH
13. Fundamental of Embedded software by Daniel W. Lewis, PHI
14. Bluetooth Technology by CSR Prabhu &A.P. Reddi, PHI
15. John B Peatman" Design with Microcontroller", Pearson education Asia, 1998
16. Burns, Alan and Wellings, Andy, " Real-Time Systems and Programming Languages", Second Edition. Harlow: Addison-Wesley-Longman,
17. 1997
18. Raymond J.A. Bhur and Donald L.Bialey, " An Introduction to real time systems: Design to networking with C/C++ ", Prentice Hall Inc. New
19. Jersey, 1999
20. Grehan Moore, and Cyliax," Real time Programming: Aguide to 32 Bit Embedded Development. Reading "Addison-Wesley-Longman, 1998
21. Heath, Steve," Embedded Systems Design ", Newnes 1997

CMOS RF CIRCUIT DESIGN

Course/Paper: 02MVL-103
MVL Semester-II

Introduction to RF design and Wireless Technology:
Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.

RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures. Direct conversion and two-step transmitters.

RF Testing

RF testing for heterodyne, Homodyne, Image reject,

Direct IF and sub sampled receivers. BJT and

MOSFET Behavior at RF **Frequencies**
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

RF Circuits Design
Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

References:

1. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998. B.Razavi "RF Microelectronics" PHI 1998
2. R. Jacob Baker, H.W. Li,D.E. Boyce " CMOS Circiut Design, layout and Simulation" PHI 1998
3. Y.P. Tsividis "Mixed Analog and Digital Devices and Technology" TMH 1996

VLSI TEST & TESTABILITY

Course/Paper: 02MVL-104
MVL Semester-II

The need for testing, the problems of digital and analog testing, Design for test, Software testing Faults in Digital circuits: General introduction, Controllability and Observability.. Faultmodels - Stuck-at faults, Bridging faults, intermittent faults

Digital test pattern generation :Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D-algorithm, Developments following Roth's D-algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits, Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing

Signatures and self test: Input compression Output compression Arithmetic, Reed-Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients ,Spectral coefficients, Coefficient test signatures ,Signature analysis and Online self test

Testability Techniques : Partitioning and ad hoc methods and Scan-path testing , Boundary scan and IEEE standard 1149.1 ,Offline built in Self Test (BIST), Hardware description languages and test Testing of Analog and Digital circuits : Testing techniques for Filters, A/D Converters, RAM, Programmable logic devices and DSP

References:

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub: Inspec/ IEE, 1999

WIRELESSS COMMUNICATION LAB

Course/Paper: 02MVL-201
MVL Semester-II

1. Measurement of antenna characteristics :
Radiation Pattern on polar plots, Beam width and Gain of main lobe for the following types of antennas.
(a) Half wave and quarter wave dipole
(b) Folded dipole
(c) Yagi UDA multiple element folded dipole
(d) Hertz Antenna
(e) End fire array and broad side array
(f) Helix antenna
(g) Para boloid reflector antenna
(h) Loop antenna
(i) Ground plane antenna
(j) Log periodic antenna
(k) Rhombus antenna
(l) Slot antenna
2. Demonstration of modeling of wire antenna using appropriate design software.
3. Simulation of antenna arrays using appropriate software.
4. Design and testing of micro strip rectangular patch antenna using appropriate software.
5. Investigate the transmission characteristics of the link and measure the gain of the microstrip patch antennas. Draw the antenna radiation diagram.
6. Radar Trainer: Working of Doppler radar, velocity of moving object, time and frequency measurement
and other applications.
7. To perform Modulation, Demodulation and BER measurement using CDMA – DSSS Trainer.
8. To establish analog/digital communication link and transmit & receive three signals (audio, video, tone) simultaneously using Satellite Communication Trainer.
9. To study GPS Receiver, establishing link between GPS satellite & GPS trainer and measure of latitude
& longitude

ALGORITHMS FOR VLSI DESIGN AUTOMATION

Course/Paper: 03MVL-101
MVL Semester-III

Logic synthesis & verification

Introductiontocombinationallogicsynthesis,BinaryDecisionDiagram,HardwaremodelsforHigh-levelsynthesis.

VLSI automation Algorithms:

Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planningalgorithmsformixedblock&celldesign.General&channelpinassignment.

Global Routing: Problem formulation, classification of global routing algorithms, Mazer outing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction

References:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
3. Rolf Drechsheler: "Evolutionary Algorithm for VLSI", Second edition
4. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

03MVL-102

PROCESS, DEVICES & CIRCUIT SIMULATION

Course/Paper: 03MVL-102
MVL Semester-III

Introduction, Main data structure & program organization, Geometrical manipulations, Ion implantation, A novel measurement technique for 2D implanted ion distributions, Introduction to partial differential equation solver, the merged multi grid method, Isothermal device modeling & simulation, Non Isothermal device modeling & simulation, hydrodynamic device modeling & simulation.

References:

1) Circuit, Device and Process Simulation: Mathematical and Numerical Aspects by Graham F. Carey (Editor), W. B. Richardson, C. S. Reed, B. Mulvaney, John Wiley & Sons; 1 edition.
2) Process and Device Simulation for MOS-VLSI Circuits, edited by P. Antognetti, D.A. Antoniadis , Robert W. Dutton, W.G. Oldham, kluwer Academic Publisher, 2000.
3)

Semester IV

DISSERTATION

Course/Paper: 4MVL-201

MVL Semester-IV

The student will submit a synopsis at the beginning of the semester for the approval from the University project committee in a specified format. Synopsis must be submitted within a two weeks. The first defense, for the dissertation work, should be held with in a one month. Dissertation Report must be submitted in a specified format to the University for evaluation purpose.